VDSL2 Multi-Processor System-on-Chip Design

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Abstract

This paper reports on the experience from a heterogeneous multi-core design for very high-rate digital subscriber line version 2 (VDSL2) modems. Between 2006 and 2008 a ten person team designed a 42 core system-on-chip, which included seven unique processor-core designs. We describe the used design tools and our design methodology based on utilizing multiple extendable processor cores. Our experience from designing such a demanding signal processing application, using the suggested methodology, proved that even a small team rapidly can design a very competitive and yet flexible system-on-chip solution.

1. Extended Abstract

Any chip design for modern communication systems developed before the standardization process is completed has the problem of balancing flexibility versus computational demand. In this paper we will look at the design of a very high-rate digital subscriber line version 2 (VDSL2) modem, developed in parallel with the standardization process.

Due to a line-code "war" the standardization of VDSL, the predecessor standard, dragged out to span more than ten years and it was not until 2006 a resolution was found. In principle this first VDSL standard was abandoned and the development of a new version, VDSL2, was started. From the beginning the basic line-code concept was decided to be using discrete multi-tone (DMT) transmission. Pieces could therefore be picked up from previous ADSL and VDSL-DMT standards, and already in 2008 the initial VDSL2 standard became published.

Upzide Labs, which had been working on IP components for VDSL since year 2000, decided in 2006 to develop a complete system-on-chip solution for VDSL2. The goal was to be ready with the design immediately when the standard would be ready. Furthermore, this needed to be accomplished with a design and development team consisting of only ten people.

Even if the basic line-code concept was decided from the start of the standardization process, almost everything else was open for discussion in the VDSL2 standardization body (ITU-T). To accommodate all potential changes in this standardization process we needed a very flexible hardware and software architecture. On the other hand the computational demand for just a single port (modem) is very high, at least 8 giga multiply-and-accumulate (MAC)

operations per second, *i.e.*, 16 GOPS. With the target of having a solution with 8 ports on a single chip there seemed to be a demand for application specific solutions which however would contradict our need for flexibility.

Our solution to this dilemma was to use a heterogeneous multi-core design based on Tensilica's extendable processor cores. This led to a solution that

- was flexible enough to accommodate almost any late specification changes
- promoted development using a very high abstraction level
- allowed a small team to develop a complex system in minimum time
- meets or beats potential rival designs in key factors like chip footprint, cost, and energy consumption

The final solution consists of five cores per port. With eight ports, a controller, and a network processor there are in total 42 cores with 7 unique core designs. Due to the economical crisis at the end of 2008 the design never was taped out. However, we believe our experience in designing one of the larger multi-core designs in Sweden to-date to be valuable to both academia and industry alike.

Our effort to develop an 8-port VDSL2 modem using the suggested design methodology shows that even a small design team can rapidly produce a very competitive and yet flexible multi-core system-on-chip solution.

1.1. Paper Outline

The paper will after an introduction of the main VDSL2 system components and key computations review various design approaches and architectures for such a system. We will especially point to one early ('93-'94) multi processor system-on-chip solution from Alcatel that was developed for ADSL and was instrumental for the company in achieving its leading position in the DSL business. Then we will present our design methodology and additional motivation for using a heterogeneous multi-core solution. After a description of the extendable processor concept of Tensilica we will describe the modularization of the application as well as the design of each unique core. When designing processors in this way, we wish to avoid synchronization on clock level between processors. Because of other design constraints (like cost and clock-rate) it is furthermore beneficial to use as simple memory types as possible (*e.g.*, avoiding dual port memories). The resulting simple interprocessor communication structure resulting from this design is presented in the paper. Finally we summarize the overall experience designing such demanding signal processing application using the suggested design methodology.